WHAT IS CLAIMED IS:

1. A processor comprising means for executing an instruction that includes a field in which a value may be assigned as a mark of enabling that a value as the result of execution of the instruction is predicted prior to or in concurrence with the execution of the instruction and a subsequent instruction is provisionally executed by using the predicted result.

2. A processor as recited in claim 1, wherein said instruction further includes a field to contain a value that designates a method of predicting a value as the result of execution of the instruction.

3. A processor as recited in claim 1, wherein said instruction further includes a field in which a value may be assigned as a mark of enabling that a value as the result of execution of the instruction is predicted and the predicted result is always used in executing a subsequent instruction, regardless of whether it is true or false.

4. A processor as recited in claim 2, wherein said instruction further includes a field in which a value may be assigned as a mark of enabling that a value as the result

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of execution of the instruction is predicted and the predicted result is always used in executing a subsequent instruction, regardless of whether it is true or false.

5. A processor provided with a cache memory to store instructions, wherein

a field in which a value may be assigned as a mark of enabling that a value as the result of execution of the instruction is predicted prior to or in concurrence with the execution of the instruction and a subsequent instruction is provisionally executed by using the predicted result is attached to each instruction stored into the cache memory.

6. A processor as recited in claim 5, wherein a field to contain a value that designates a method of predicting a value as the result of execution of the instruction is further attached to each instruction stored into the cache memory.

7. A processor as recited in claim 5, wherein the processor includes means for updating the values existing in the fields provided for each instruction stored into the cache memory, depending on whether the predicted value as the result of execution of the instruction is true or false.

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8. A processor as recited in claim 5, wherein a field in which a value may be assigned as a mark of enabling that a value as the result of execution of the instruction is predicted and the predicted result is always used in executing a subsequent instruction, regardless of whether it is true or false, is further attached to each instruction stored into the cache memory.

9. A processor comprising:

a cache memory to store an instruction to which a first field is attached, the first field in which a value may be assigned as a mark of enabling that a value as the result of execution of the instruction is predicted prior to or in concurrence with the execution of the instruction and a subsequent instruction is provisionally executed by using the predicted result;

execution means which fetches an instruction from the cache memory and executes the instruction;

value prediction means which predicts a value as the result of execution of an instruction prior to or in concurrence with the execution of the instruction;

gating means which enables outputting the result of prediction made by said value prediction means only for an instruction with said mark contained in its first field so as to be used in executing a subsequent instruction; and

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storage means which stores the predicted result of execution of an instruction passed through said gating means and the result of executing the instruction by said execution means for further processing.

10. A processor as recited in claim 9, further comprising means for determining a match/mismatch between the result of prediction made by said value prediction means and the result of instruction execution by said execution means for each instruction to be executed.

11. A processor as recited in claim 10, wherein a second field is further attached to an instruction to be stored into said cache memory, the second field to contain a value that designates a method of predicting the result of execution of the instruction, and said value prediction means predicts the result of execution of each instruction by using the prediction method designated by the contents of the second field of the instruction.

12. A processor as recited in claim 11, further comprising means for updating the contents of the first field or the second field of an instruction stored in the cache memory if the means for determining a match/mismatch has determined a mismatch for the instruction.

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13. A processor as recited in claim 10, wherein a third field is attached to an instruction to be stored into said cache memory, the third field in which a value may be assigned as a mark of enabling that the result of prediction made by said value prediction means is always used in executing a subsequent instruction, regardless of whether it is true or false,

wherein the result of prediction for an instruction without the mark contained in the third field, made by said prediction means, and the result of execution of a subsequent instruction by using the result of prediction are nullified when said means for determining a match/mismatch has determined a mismatch for the instruction, whereas the result of prediction for an instruction with the mark contained in the third field, made by said prediction means, is always taken to be valid.